**Project Report- EE287**

**Inverse Fast Fourier Transform**

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We have used three state machines for the entire 32 point inverse fast fourier transform. One state machine is for collecting the inputs and giving them to the butterfly module.

Second state machine is for collecting the output values from the butterfly structure and storing in memory.

Third state machine is for giving the final answers to the output ports by using a pushout signal.

The design passes the RTL level simulations, design is synthezised with 4ns clock period and also passes the gate level simulations without any timing violations.